2-Bit, Dual Supply, Bus Transceiver With Configurable Level-Shifting and Translation

1 FEATURES

- **V_{CC} Isolation Feature: If Either V_{CC} Input is at GND, Both Ports are in The High-Impedance State**
- **Dual Supply Rail Design**
- **I/Os Are 4.6V Over Voltage Tolerant**
- **I_{off} Supports Partial Power-Down-Mode Operation**
- **Typical Max Data Rates**
  - **380 Mbps (1.8 V to 3.3 V Translation)**
  - **200 Mbps (<1.8 V to 3.3 V Translation)**
  - **200 Mbps (Translate to 2.5 V or 1.8 V)**
- **Extended Temperature: -40°C to 125°C**

2 APPLICATIONS

- **Smartphones**
- **Servers**
- **Desktop PCs and Notebooks**
- **Other Portable Devices**

3 DESCRIPTIONS

This 2-bit non-inverting bus transceiver uses two separate configurable power-supply rails. The A ports are designed to track V_{CCA} and accepts any supply voltage from 1.2 V to 3.6 V. The B ports are designed to track V_{CCB} and accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation and level-shifting between any of the 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V voltage nodes.

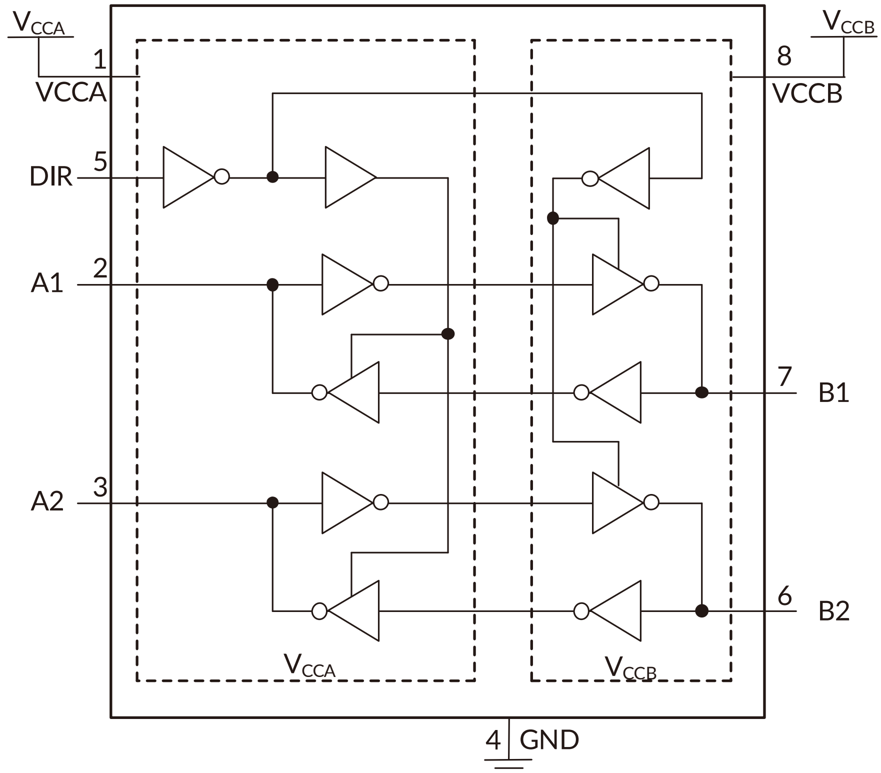
The RS74AVC2T45 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR pin) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess leakage current on the internal CMOS structure.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
RS74AVC2T45	VSSOP8	2.00mm×2.30mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 FUNCTIONAL BLOCK DIAGRAM



Function Table (Each Transceiver)

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

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5 REVISION HISTORY

Note: Page numbers for previous revisions may different from page numbers in the current version.

VERSION	Change Date	Change Item
A.1	2025/06/20	Initial version completed

6 PACKAGE/ORDERING INFORMATION (1)

PRODUCT	ORDERING NUMBER	TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE MARKING (2)	MSL(3)	PACKAGE OPTION
RS74AVC2T45	RS74AVC2T45XVS8	-40°C ~125°C	VSSOP8	V2T	MSL3	Tape and Reel, 3000

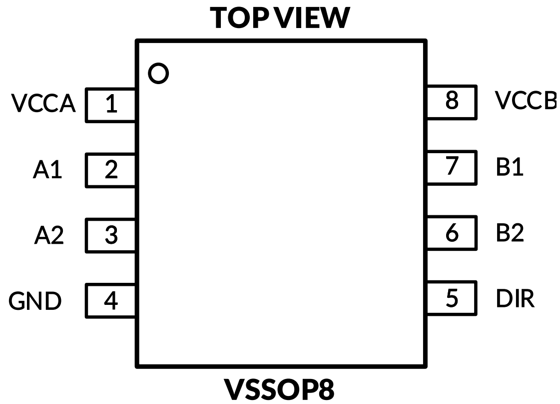
NOTE:

(1) This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the right-hand navigation.

(2) There may be additional marking, which relates to the lot trace code information (data code and vendor code), the logo or the environmental category on the device.

(3) RUNIC classify the MSL level with using the common preconditioning setting in our assembly factory conforming to the JEDEC industrial standard J-STD-20F. Please align with RUNIC if your end application is quite critical to the preconditioning setting or if you have special requirement.

7 PIN CONFIGURATIONS



PIN DESCRIPTION

PIN		TYPE (1)	FUNCTION
NAME	NO.		
VCCA	1	-	Supply Voltage A
VCCB	8	-	Supply Voltage B
GND	4	-	Ground
A1	2	I/O	Output or input depending on state of DIR. Output level depends on V_{CCA}.
A2	3	I/O	Output or input depending on state of DIR. Output level depends on V_{CCA}.
B1	7	I/O	Output or input depending on state of DIR. Output level depends on V_{CCB}.
B2	6	I/O	Output or input depending on state of DIR. Output level depends on V_{CCB}.
DIR	5	I	Direction Pin, Connect to GND or to VCCA

(1) I=input, O=output, I/O=input and output.

8 SPECIFICATIONS

8.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted) (1)

SYMBOL	PARAMETER		MIN	MAX	UNIT
V_{CCA}	Supply Voltage Range		-0.5	4.6	V
V_{CCB}	Supply Voltage Range		-0.5	4.6	V
V_I	Input Voltage Range (2)	I/O ports (A port)	-0.5	4.6	V
		I/O ports (B port)	-0.5	4.6	
		Control inputs	-0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state (2)	A port	-0.5	4.6	V
		B port	-0.5	4.6	
V_O	Voltage range applied to any output in the high or low state (2) (3)	A port	-0.5	$V_{CCA}+0.5$	V
		B port	-0.5	$V_{CCB}+0.5$	
I_{IK}	Input clamp current	$V_I<0$		-50	mA
I_{OK}	Output clamp current	Vo<0		-50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCA}, V_{CCB} or GND			±100	mA
T_{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.

8.2 ESD Ratings

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-Body Model (HBM), JEDEC EIA/JESD22-A114	±2000	V
		Charged-Device Model (CDM), ANSI/ESDA/JEDEC JS-002-2022	±1000	V
		Machine Model (MM), JESD22-A115C (2010)	±100	V

ESD SENSITIVITY CAUTION

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.3 Recommended Operating Conditions

			V_{CCI} (1)	V_{CCO} (2)	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.2	3.6	V
V_{CCB}	Supply voltage				1.2	3.6	V
V_{IH}	HIGH-level input voltage	Data inputs (4)	1.2 V to 1.95 V		$V_{CCI} \times 0.65$		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	LOW-level input voltage	Data inputs (4)	1.2 V to 1.95 V			$V_{CCI} \times 0.35$	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_{IH}	HIGH-level input voltage	DIR (referenced to V_{CCA}) (5)	1.2 V to 1.95 V		$V_{CCA} \times 0.65$		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	LOW-level input voltage	DIR (referenced to V_{CCA}) (5)	1.2 V to 1.95 V			$V_{CCA} \times 0.35$	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.2 V		-3	mA
				1.4 V to 1.6 V		-6	
				1.65 V to 1.95 V		-8	
				2.3 V to 2.7 V		-9	
				3 V to 3.6 V		-12	
I_{OL}	Low-level output current			1.2 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				-40	125	°C

(1) V_{CCI} is the voltage associated with the input port supply V_{CCA} or V_{CCB}.
(2) V_{CCO} is the voltage associated with the output port supply V_{CCA} or V_{CCB}.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = $V_{CCI} \times 0.65$ V, V_{IL} max = $V_{CCI} \times 0.35$ V.
(5) For V_{CCA} values not specified in the data sheet, V_{IH} min = $V_{CCA} \times 0.65$ V, V_{IL} max = $V_{CCA} \times 0.35$ V.

8.4 Electrical Characteristics

All typical limits apply over T_A = 25°C, and all maximum and minimum limits apply over T_A = −40°C to 125°C (unless otherwise noted). (1) (2)

PARAMETER		TEST CONDITIONS		MIN(3)	TYP(4)	MAX(3)	UNIT
V_{OH}		I_{OH}=−100 µA; V_{CCA}=1.2 V to 3.6 V; V_{CCB}=1.2 V to 3.6 V; V_I=V_{IH}		V_{CCO}-0.2			V
		I_{OH}=−3 mA; V_{CCA}=1.2 V; V_{CCB}=1.2 V; V_I=V_{IH}			0.95		
		I_{OH}=−6 mA; V_{CCA}=1.4 V; V_{CCB}=1.4 V; V_I=V_{IH}		0.9			
		I_{OH}=−8 mA; V_{CCA}=1.65 V; V_{CCB}=1.65 V; V_I=V_{IH}		1.2			
		I_{OH}=−9 mA; V_{CCA}=2.3 V; V_{CCB}=2.3 V; V_I=V_{IH}		1.75			
		I_{OH}=−12 mA; V_{CCA}=3.0 V; V_{CCB}=3.0 V; V_I=V_{IH}		2.3			
V_{OL}		I_{OL}=100 µA; V_{CCA}=1.2 V to 3.6 V; V_{CCB}=1.2 V to 3.6 V; V_I=V_{IL}				0.2	V
		I_{OL}=3 mA; V_{CCA}=1.2 V; V_{CCB}=1.2 V; V_I=V_{IL}			0.25		
		I_{OL}=6 mA; V_{CCA}=1.4 V; V_{CCB}=1.4 V; V_I=V_{IL}				0.35	
		I_{OL}=8 mA; V_{CCA}=1.65 V; V_{CCB}=1.65 V; V_I=V_{IL}				0.45	
		I_{OL}=9 mA; V_{CCA}=2.3 V; V_{CCB}=2.3 V; V_I=V_{IL}				0.55	
		I_{OL}=12 mA; V_{CCA}=3.0 V; V_{CCB}=3.0 V; V_I=V_{IL}				0.7	
I_I (DIR input)		V_I=V_{CCA} or GND; V_{CCA} =1.2 V to 3.6 V; V_{CCB}=1.2 V to 3.6 V	T_A = 25°C		±0.002	±1	µA
			T_A = −40°C to 125°C			±2	
I_{off}	A port	V_I or V_O=0 V to 3.6 V; V_{CCA} = 0 V; V_{CCB} = 0 V to 3.6 V	T_A = 25°C		±0.001	±1	µA
			T_A = −40°C to 125°C			±5	
	B port	V_I or V_O=0 V to 3.6 V; V_{CCA} =0 V to 3.6 V; V_{CCB} = 0 V	T_A = 25°C		±0.002	±1	
			T_A = −40°C to 125°C			±5	
I_{OZ} (5)	A port & B port	V_O=V_{CCO} or GND; V_I=V_{CCI} or GND; $\overline{OE}$=V_{IH}; V_{CCA}=3.6 V; V_{CCB}=3.6 V	T_A = 25°C		±0.05	±1	µA
			T_A = −40°C to 125°C			±5	
I_{CCA}		V_I=V_{CCI} or GND, I_O=0	V_{CCA}=1.2V to 3.6V; V_{CCB}=1.2V to 3.6V			7	µA
			V_{CCA}=0V; V_{CCB}=3.6V			-2	
			V_{CCA}=3.6V; V_{CCB}=0V			7	
I_{CCB}		V_I=V_{CCI} or GND, I_O=0	V_{CCA}=1.2V to 3.6V; V_{CCB}=1.2V to 3.6V			7	µA
			V_{CCA}=0V; V_{CCB}=3.6V			7	
			V_{CCA}=3.6V; V_{CCB}=0V			-2	
I_{CCA}+I_{CCB}		V_I=V_{CCI} or GND, I_O=0; V_{CCA}=1.2 V to 3.6 V; V_{CCB}=1.2 V to 3.6 V				14	µA
C_i	Control inputs	V_I = 3.3 V or GND; V_{CCA} = 3.3 V; V_{CCB} = 3.3 V			1.5	4.5	pF
C_{io}	A or B port	V_O = 3.3 V or GND; V_{CCA} = 3.3 V; V_{CCB} = 3.3 V			2.5	7	pF

(1) V_{CCO} is the voltage associated with the output port supply V_{CCA} or V_{CCB}.
(2) V_{CCI} is the voltage associated with the input port supply V_{CCA} or V_{CCB}.
(3) Limits are 100% production tested at 25°C. Limits over the operating temperature range are ensured through correlations using statistical quality control (SQC) method.
(4) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration.
(5) For I/O ports, the parameter I_{OZ} includes the input leakage current.

8.5 Switching Characteristics, V_{CCA}=1.2 V

over recommended operating free-air temperature range.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}=1.2V	V_{CCB}=1.5V ±0.1V	V_{CCB}=1.8V ±0.15V	V_{CCB}=2.5V ±0.2V	V_{CCB}=3.3V ±0.3V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t_{PLH}	A	B	20.6	15.8	14.1	12.5	12.2	ns
t_{PHL}			16.3	13.0	12.1	11.1	11.1	
t_{PLH}	B	A	20.3	17.3	15.7	14.4	14.1	ns
t_{PHL}			16.3	13.3	12.0	10.4	9.5	
t_{PZH}	$\overline{OE}$	A	24.0	23.0	23.3	23.8	22.8	ns
t_{PZL}			20.0	19.8	19.5	19.3	19.3	
t_{PZH}	$\overline{OE}$	B	25.3	21.0	19.8	16.8	15.3	ns
t_{PZL}			22.3	18.3	16.5	15.3	14.3	
t_{PHZ}	$\overline{OE}$	A	19.3	18.5	17.8	18.5	19.5	ns
t_{PLZ}			17.8	17.0	16.3	16.3	16.8	
t_{PHZ}	$\overline{OE}$	B	17.8	16.3	15.3	14.5	14.0	ns
t_{PLZ}			18.0	17.3	16.0	16.0	15.8	

8.6 Switching Characteristics, V_{CCA}=1.5 V ± 0.1 V

over recommended operating free-air temperature range.

PARA METER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}=1.2V	V_{CCB}=1.5V ±0.1V		V_{CCB}=1.8V ±0.15V		V_{CCB}=2.5V ±0.2V		V_{CCB}=3.3V ±0.3V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	17.1	6.2	14.6	5.2	12.5	4.4	10.2	4.0	9.5	ns
t_{PHL}			12.2	4.7	11.4	4.0	9.3	3.5	8.9	3.3	7.7	
t_{PLH}	B	A	15.5	6.2	15.2	5.5	13.1	4.7	11.5	4.5	11.2	ns
t_{PHL}			13.1	5.0	12.2	4.2	10.4	3.5	8.4	3.1	7.6	
t_{PZH}	$\overline{OE}$	A	20.5	10.4	24.7	8.3	25.0	6.8	25.0	6.3	24.7	ns
t_{PZL}			15.0	6.6	18.1	6.3	18.4	5.5	18.4	5.3	18.1	
t_{PZH}	$\overline{OE}$	B	23.5	9.9	25.9	10.0	20.6	10.0	16.9	9.9	15.6	ns
t_{PZL}			17.3	7.3	16.6	7.4	15.6	7.4	13.8	7.3	13.1	
t_{PHZ}	$\overline{OE}$	A	12.0	6.8	13.8	5.8	14.1	5.6	13.8	5.3	14.1	ns
t_{PLZ}			14.0	6.4	17.2	6.0	16.6	5.9	16.3	5.6	15.9	
t_{PHZ}	$\overline{OE}$	B	14.8	5.5	16.9	5.6	14.4	5.5	14.1	5.6	13.1	ns
t_{PLZ}			13.5	6.9	15.9	6.6	15.0	6.5	14.7	6.4	14.1	

8.7 Switching Characteristics, V_{CCA}=1.8 V ± 0.15 V

over recommended operating free-air temperature range.

PARA METER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}=1.2V	V_{CCB}=1.5V ±0.1V		V_{CCB}=1.8V ±0.15V		V_{CCB}=2.5V ±0.2V		V_{CCB}=3.3V ±0.3V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	15.3	5.4	13.0	4.3	10.5	3.4	7.9	3.1	7.4	ns
t_{PHL}			10.7	4.0	9.8	3.3	8.2	2.8	6.8	2.5	6.3	
t_{PLH}	B	A	13.7	5.3	13.1	4.6	11.0	3.9	9.5	3.5	8.9	ns
t_{PHL}			11.8	4.3	10.6	3.7	8.7	2.9	6.9	2.6	6.2	
t_{PZH}	$\overline{OE}$	A	14.0	9.6	17.5	7.5	17.5	6.3	17.2	5.4	17.2	ns
t_{PZL}			11.3	5.8	13.8	5.0	14.1	4.3	13.8	4.0	13.4	
t_{PZH}	$\overline{OE}$	B	22.8	7.0	24.1	7.0	18.8	6.9	15.6	6.9	13.4	ns
t_{PZL}			15.3	5.5	14.4	5.6	12.5	5.5	10.6	5.4	10.0	
t_{PHZ}	$\overline{OE}$	A	13.0	6.3	15.6	5.0	15.9	4.6	15.0	4.3	15.0	ns
t_{PLZ}			11.3	5.3	13.1	4.6	13.4	4.6	13.1	4.5	12.2	
t_{PHZ}	$\overline{OE}$	B	13.3	6.3	15.6	6.4	12.5	6.0	11.6	6.0	10.6	ns
t_{PLZ}			11.8	5.3	13.1	5.4	11.6	5.3	11.6	4.9	11.3	

8.8 Switching Characteristics, V_{CCA}=2.5 V ± 0.2 V

over recommended operating free-air temperature range.

PARA METER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}=1.2V	V_{CCB}=1.5V ±0.1V		V_{CCB}=1.8V ±0.15V		V_{CCB}=2.5V ±0.2V		V_{CCB}=3.3V ±0.3V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	14.4	4.8	11.6	3.8	9.5	3.1	7.5	2.5	6.3	ns
t_{PHL}			9.0	3.1	7.9	2.6	6.3	2.0	5.1	2.0	4.8	
t_{PLH}	B	A	12.6	4.5	11.0	3.8	9.2	3.0	7.2	2.7	6.8	ns
t_{PHL}			10.8	3.8	9.7	3.2	7.8	2.6	6.0	2.2	5.2	
t_{PZH}	$\overline{OE}$	A	9.8	9.4	12.2	7.0	12.5	5.5	11.9	4.9	11.9	ns
t_{PZL}			8.8	4.9	10.6	4.3	10.9	3.8	10.9	3.4	10.6	
t_{PZH}	$\overline{OE}$	B	20.8	4.9	23.4	5.0	17.5	4.8	13.8	4.8	12.2	ns
t_{PZL}			13.3	4.3	12.2	4.4	10.6	4.4	9.4	4.3	8.4	
t_{PHZ}	$\overline{OE}$	A	8.8	5.6	9.7	5.0	10.6	4.6	10.0	4.0	10.0	ns
t_{PLZ}			9.8	4.9	11.9	4.3	11.6	4.6	11.9	4.3	10.9	
t_{PHZ}	$\overline{OE}$	B	12.5	3.9	14.1	4.3	12.5	4.0	11.6	4.0	10.0	ns
t_{PLZ}			11.3	4.8	12.2	4.6	10.6	4.8	11.6	4.4	10.6	

8.9 Switching Characteristics, V_{CCA}=3.3 V ± 0.3 V

over recommended operating free-air temperature range.

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCB}=1.2V	V_{CCB}=1.5V ±0.1V		V_{CCB}=1.8V ±0.15V		V_{CCB}=2.5V ±0.2V		V_{CCB}=3.3V ±0.3V		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	14.3	4.7	11.4	3.7	8.7	2.8	6.7	2.4	5.9	ns
t_{PHL}			8.6	2.8	7.2	2.5	5.9	1.8	4.4	1.6	4.3	
t_{PLH}	B	A	12.3	4.2	10.4	3.3	8.3	2.7	6.3	2.5	6.3	ns
t_{PHL}			11.1	3.7	9.2	2.9	7.4	2.3	5.5	1.8	4.4	
t_{PZH}	$\overline{OE}$	A	7.8	9.1	9.7	7.0	9.7	5.4	9.7	5.0	9.7	ns
t_{PZL}			7.8	4.4	9.7	3.6	10.0	3.6	10.0	3.0	9.7	
t_{PZH}	$\overline{OE}$	B	22.0	3.9	22.8	3.9	17.5	3.9	13.4	3.9	12.5	ns
t_{PZL}			13.5	3.9	10.9	4.0	9.1	4.0	9.1	3.9	7.5	
t_{PHZ}	$\overline{OE}$	A	8.0	5.8	10.0	4.5	10.3	4.1	10.0	4.0	10.6	ns
t_{PLZ}			8.0	4.1	10.3	3.3	10.9	2.6	10.3	2.4	10.3	
t_{PHZ}	$\overline{OE}$	B	12.0	4	14.7	4.1	11.3	4.0	10.3	4.3	10.0	ns
t_{PLZ}			9.8	4.1	10.3	4.4	8.1	4.1	6.6	4.1	5.9	

8.10 Operating Characteristics

T_A=25°C

PARAMETER			TEST CONDITIONS	V_{CCA}= V_{CCB}=1.2V	V_{CCA}= V_{CCB}=1.5V	V_{CCA}= V_{CCB}=1.8V	V_{CCA}= V_{CCB}=2.5V	V_{CCA}= V_{CCB}=3.3V	UNIT
				TYP	TYP	TYP	TYP	TYP	
C_{pdA}(1)	A to B	Outputs enabled	C_L=0, f=10MHz, t_r = t_f = 1ns	2	2	2	1.5	2.5	pF
		Outputs disable		1	1	1	0.5	1	
	B to A	Outputs enabled		12	13	13	14	15	
		Outputs disable		1	1	1	1	1.5	
C_{pdB}(1)	A to B	Outputs enabled	C_L=0, f=10MHz, t_r = t_f = 1ns	12	13	13	14	15	pF
		Outputs disable		1	1	1	1	1.5	
	B to A	Outputs enabled		2	2	2	2	2.5	
		Outputs disable		1	1	1	0.5	1	

(1) Power dissipation capacitance per transceiver.

8.11 Typical Characteristics

NOTE: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only.

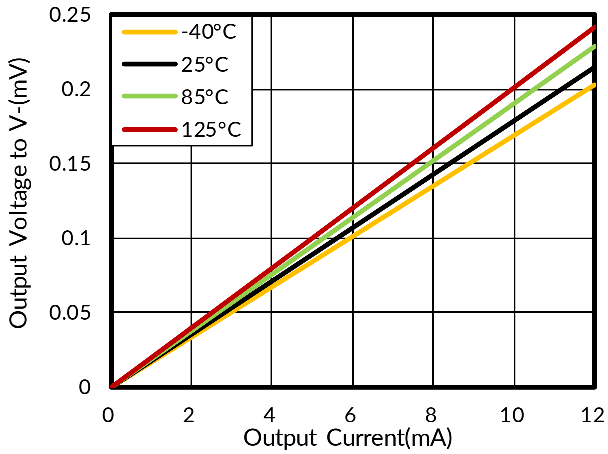


Figure 1. Output Voltage Low vs Output Current, 3V

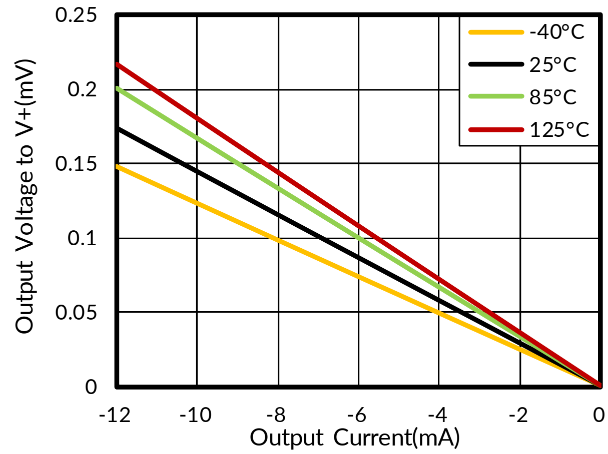
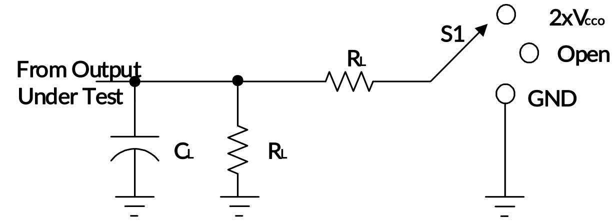


Figure 2. Output Voltage High vs Output Current, 3V

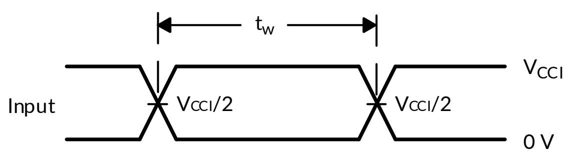
9 PARAMETER MEASUREMENT INFORMATION



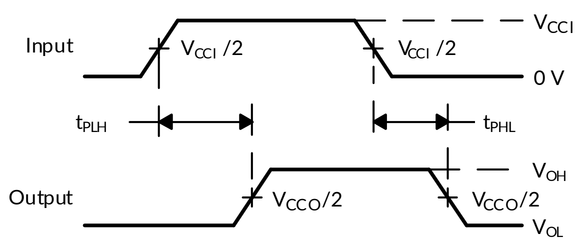
LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 x V_{CCO}
t_{PHZ}/t_{PZH}	GND

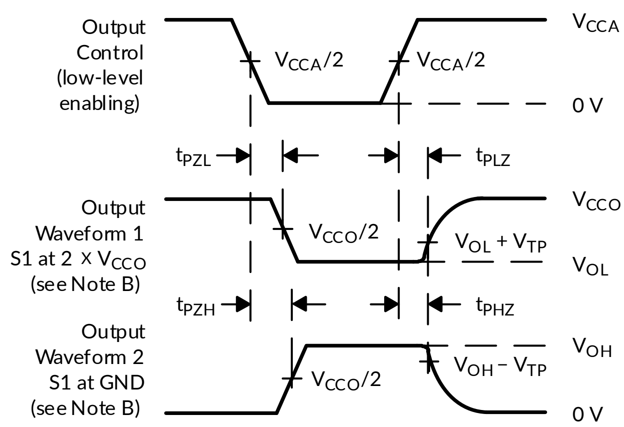
V_{CC}	C_L	R_L	V_{TP}
1.2V	15pF	2kΩ	0.1V
1.5V±0.1V	15pF	2kΩ	0.1V
1.8V±0.15V	15pF	2kΩ	0.15V
2.5V±0.2V	15pF	2kΩ	0.15V
3.3V±0.3V	15pF	2kΩ	0.3V



VOLTAGE WAVEFORMS
PULSE DURA TION



VOLTAGE WAVEFORMS
PROPAGA TION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤10 MHz, Z_O = 50Ω, dv/dt≥1V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.

Figure 3. Load Circuit and Voltage Waveforms

10 DETAILED DESCRIPTION

10.1 Overview

This dual-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} and accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB} and accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation and level-shifting between any of the 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V voltage nodes.

The RS74AVC2T45 is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess internal leakage of the CMOS.

The RS74AVC2T45 is designed so that the DIR input is powered by supply voltage from VCCA.

This device is fully specified for partial-power-down applications using off output current (I_{off}). The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either VCC input is at GND, both ports are put in a high-impedance state. This will prevent a false high or low logic being presented at the output.

10.2 Feature Description

10.2.1 VCC Isolation

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} are at GND, both ports will be in a high-impedance state (I_{OZ} shown in Electrical Characteristics). This prevents false logic levels from being presented to either bus.

10.2.2 2-Rail Design

Fully configurable 2-rail design allows each port to operate over the full 1.2 V to 3.6 V power-supply range.

10.2.3 IO Ports are 4.6V Tolerant

The IO ports are up to 4.6 V tolerant.

10.2.4 Partial-Power-Down Mode

This device is fully specified for partial-power-down applications using off output current (I_{off}). The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

11 APPLICATION AND IMPLEMENTATION

Information in the following applications sections is not part of the RUNIC component specification, and RUNIC does not warrant its accuracy or completeness. RUNIC's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

11.1 Application Information

The RS74AVC2T45 is used to shift IO voltage levels from one voltage domain to another. Bus A and bus B have independent power supplies, and a direction pin is used to control the direction of data flow. Unused data ports must not be floating; tie the unused port input and output to ground directly.

11.1.1 Enable Times

Calculate the enable times for the RS74AVC2T45 using the following formulas:

- t_{PZH} (DIR to A) = t_{PLZ} (DIR to B) + t_{PLH} (B to A)
- t_{PZL} (DIR to A) = t_{PHZ} (DIR to B) + t_{PHL} (B to A)
- t_{PZH} (DIR to B) = t_{PLZ} (DIR to A) + t_{PLH} (A to B)
- t_{PZL} (DIR to B) = t_{PHZ} (DIR to A) + t_{PHL} (A to B)

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the RS74AVC2T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting it with an input. After the B port has been disabled, an input signal applied to it appears on the corresponding A port after the specified propagation delay.

11.2 Typical Application

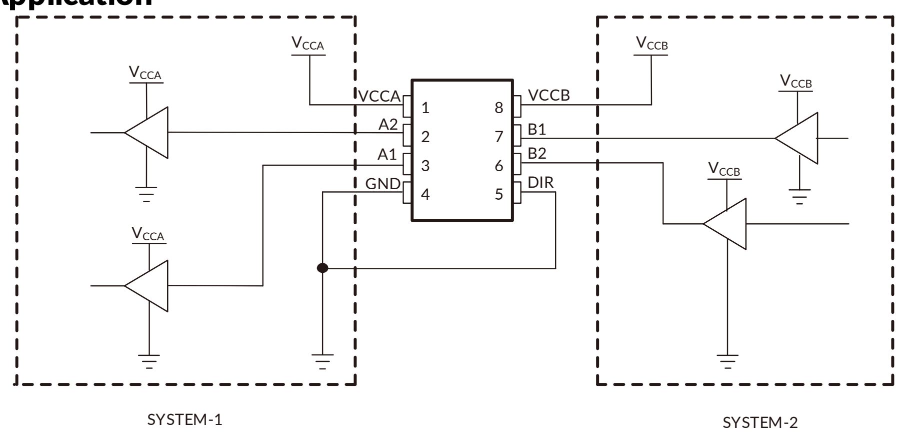


Figure 4. Unidirectional Logic Level-Shifting Application

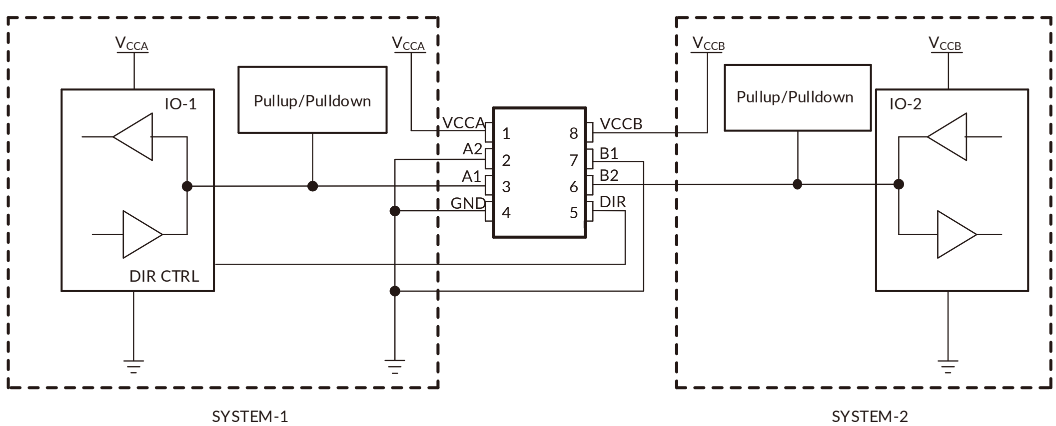


Figure 5. Bidirectional Logic Level-Shifting Application

12 POWER SUPPLY RECOMMENDATIONS

A proper power-up sequence always should be followed to avoid excessive current on the supply pin, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

1. Connect ground before any supply voltage is applied.
2. Power up V_{CCA}.
3. V_{CCB} can be ramped up along with or after V_{CCA}.

Table 1. Typical Total Static Power Consumption (I_{CCA} + I_{CCB})

V_{CCB}	V_{CCA}						UNIT
	0V	1.2V	1.5V	1.8V	2.5V	3.3V	
0V	0	<0.5	<0.5	<0.5	<0.5	<0.5	μA
1.2V	<0.5	<1	<1	<1	<1	1	
1.5V	<0.5	<1	<1	<1	<1	1	
1.8V	<0.5	<1	<1	<1	<1	<1	
2.5V	<0.5	1	<1	<1	<1	<1	
3.3V	<0.5	1	<1	<1	<1	<1	

13 LAYOUT

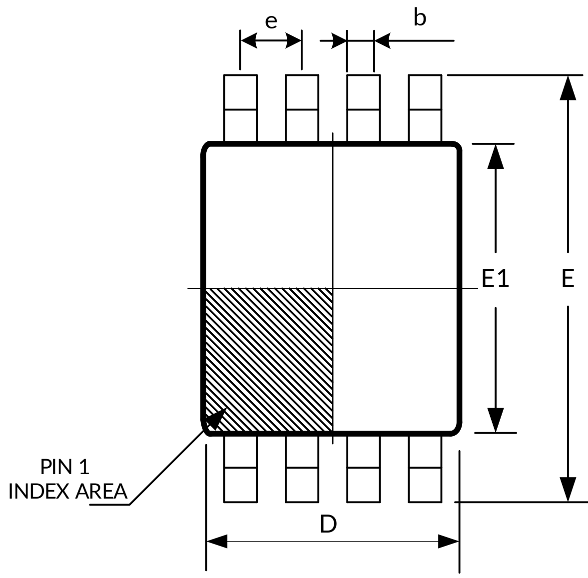
13.1 Layout Guidelines

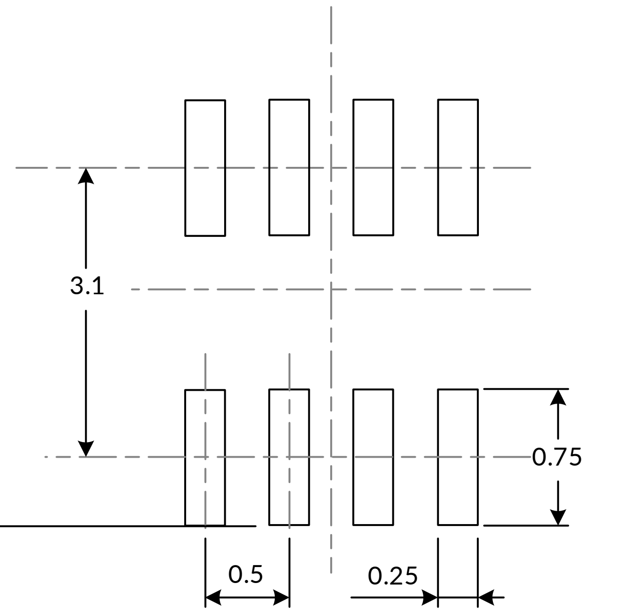
To ensure reliability of the device, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies. Place the capacitors as close as possible to the VCCA, VCCB pin and GND pin.
- Short trace lengths should be used to avoid excessive loading.

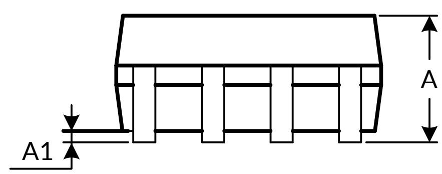
14 PACKAGE OUTLINE DIMENSIONS

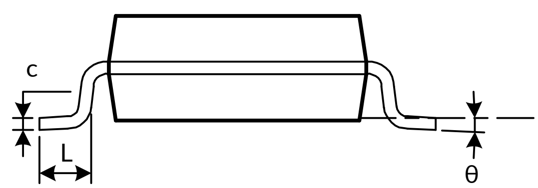
VSSOP8 (3)





RECOMMENDED LAND PATTERN (Unit: mm)





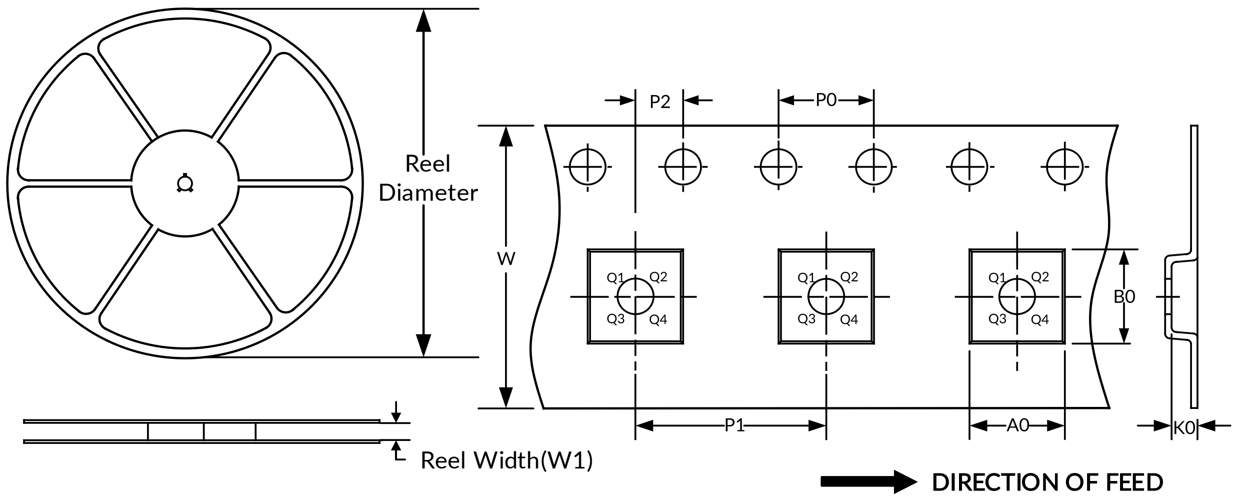
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A (1)	0.600	0.900	0.024	0.085
A1	0.000	0.100	0.000	0.004
b	0.170	0.250	0.007	0.010
c	0.100	0.200	0.004	0.008
D (1)	1.900	2.100	0.075	0.083
e	0.500 (BSC) (2)		0.020 (BSC) (2)	
E	3.000	3.200	0.118	0.126
E1 (1)	2.200	2.400	0.087	0.095
L	0.200	0.350	0.008	0.014
θ	0°	6°	0°	6°

NOTE:

1. Plastic or metal protrusions of 0.15mm maximum per side are not included.
2. BSC (Basic Spacing between Centers), "Basic" spacing is nominal.
3. This drawing is subject to change without notice.

15 TAPE AND REEL INFORMATION

REEL DIMENSIONS **TAPE DIMENSION**



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
VSSOP8	7”	9.5	2.25	3.35	1.40	4.0	4.0	2.0	8.0	Q3

NOTE:
1. All dimensions are nominal.
2. Plastic or metal protrusions of 0.15mm maximum per side are not included.

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